(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) Publication number : **0 604 166 A1**

(12) EUROPEAN PATENT APPLICATION

(21) Application number : **93310316.0**

(51) Int. Cl.^{5} : **H04B 1/20**, H04L 12/40

(22) Date of filing : **20.12.93**

(30) Priority : **21.12.92 JP 340405/92**
21.10.93 JP 263651/93

(43) Date of publication of application :
29.06.94 Bulletin 94/26

(84) Designated Contracting States :
DE GB NL

(71) Applicant : **SONY CORPORATION**
7-35, Kitashinagawa 6-chome
Shinagawa-ku
Tokyo (JP)

(72) Inventor : **Osakabe, Yoshio, c/o Sony Corporation**
7-35 Kitashinagawa 6-chome,
Shinagawa-Ku
Tokyo (JP)
Inventor : **Yamazaki, Hiroshi, c/o Sony Corporation**
7-35 Kitashinagawa 6-chome,
Shinagawa-Ku
Tokyo (JP)
Inventor : **Sugiyama, Kouichi, c/o Sony Corporation**
7-35 Kitashinagawa 6-chome,
Shinagawa-Ku
Tokyo (JP)
Inventor : **Tanaka, Shigeo, c/o Sony Corporation**
7-35 Kitashinagawa 6-chome,
Shinagawa-ku
Tokyo (JP)
Inventor : **Katsuyama, Akira, Sony Corporation**
7-35 Kitashinagawa 6-chome,
Shinagawa-ku
Tokyo (JP)
Inventor : **Kusagaya, Yasuo, c/o Sony Corporation**
7-35 Kitashinagawa 6-chome,
Shinagawa-ku
Tokyo (JP)
Inventor : **Kotabe, Noriko, c/o Sony Corporation**
7-35 Kitashinagawa 6-chome,
Shinagawa-ku
Tokyo (JP)
Inventor : **Sato, Makoto, c/o Sony Corporation**
7-35 Kitashinagawa 6-chome,
Shinagawa-ku
Tokyo (JP)

(74) Representative : **Ayers, Martyn Lewis Stanley**
J.A. KEMP & CO.
14 South Square
Gray's Inn
London WC1R 5LX (GB)

(54) Communication system and communication devices having lock function.

(57) There is disclosed a communication system using a bi-directional bus, which comprises a plurality of devices (e.g., TV image receiver or video tape recorder, etc.) connected to each other. Each device comprises a transmit signal formation unit having a frame structure consisting of an address field for specifying addresses of devices between which communication is to be carried out, a control field for specifying whether communication is to be carried out in the state where device on the receiving side is locked or in the state where that device is not locked, and a data field for specifying data to be transmitted. In transmitting data to be transmitted having a data quantity greater than data capacity of the data field in a manner divided into a plurality of frames, an indication to lock device on the receiving side is given to control field of a frame transmitted first, and an indication not to lock that device is given to control field of a frame transmitted last. The transmit signal thus indicated is transmitted through the bi-directional bus by a bus output unit. In addition, there are also disclosed a transmitting method, a receiving method and a communication method, which can be applied to such a bi-directional bus system.

EP 0 604 166 A1

P1 (VTR → TV)

HEADER	HEADER
MASTER ADDRESS BITS	VTR
SLAVE ADDRESS BITS	TV
CONTROL BITS	DATA/ LOCK
TEXT HEADER	"AB" h
HDOPR	SUB-DEVICE → DEVICE
SSDA	VIDEO DECK
DTATR	"20" h
BYTE	"2A" h
OPR1	"20" h
OPR2	"22" h
OPR3	"21" h
DATA #9 ⋮ DATA #16	DATA ⋮ DATA

P2 (VTR → TV)

HEADER	HEADER
MASTER ADDRESS BITS	VTR
SLAVE ADDRESS BITS	TV
CONTROL BITS	DATA/ NON-LOCK
TEXT HEADER	"AB" h
HDOPR	SUB-DEVICE → DEVICE
SSDA	VIDEO DECK
DTATR	"20" h
BYTE	"27" h
DATA #6 ⋮ DATA #13	DATA ⋮ DATA

P3 (VDP → TV)

HEADER	HEADER
MASTER ADDRESS BITS	VDP
SLAVE ADDRESS BITS	TV
CONTROL BITS	DATA/ NON-LOCK
TEXT HEADER	"AB" h
HDOPR	SUB-DEVICE → DEVICE
SSDA	VIDEO PLAYER
DTATR	"20" h
BYTE	"2A" h
OPR1	"20" h
OPR2	"22" h
OPR3	"21" h
DATA #9 ⋮ DATA #16	DATA ⋮ DATA

FIG.13

This invention relates to a transmitting method, a receiving method, a communication method, and a bi-directional bus system, which are used in a system in which devices, e.g., a television image receiver or a video tape recorder, etc. are connected to each other by using a bi-directional bus to control, from other devices, sub-devices, e.g., a monitor image receiver, a TV tuner, or a video deck, etc. included in the devices, or to display the operating states, etc. of other devices on the television image receiver.

In recent years, there have been popularly used systems in which a plurality of pieces of audio equipment or visual equipment (hereinafter referred to as AV equipment) are connected by means of video signal lines or audio signal lines (hereinafter referred to as AV signal lines).

In such AV systems, equipment is connected by means of a system control bus (hereinafter simply referred to as a bi-directional bus) in addition to the above-described AV signal lines to control respective pieces of equipment. In a practical sense, for Audio, Video and audiovisual systems, a Domestic Digital Bus (hereinafter referred to as D2B) standardized by the so-called publication 1030 of IEC, a Home Bus System (hereinafter referred to as HBS) standardized by the ET-2101 of EIAJ, and the like are known. Through the bi-directional bus, other devices may be controlled from equipment (devices), e.g., a television image receiver, a video tape recorder, and a video deck player (hereinafter respectively referred to as TV, VTR, VDP), etc., and sub-devices, e.g., a monitor image receiver (TV monitor), a TV tuner, a video deck, or an amplifier, etc. included in other devices are controlled from devices. Further, through the bi-directional bus, data for displaying, on a TV monitor, e.g., the operating state (status) of a device or sub-device is transmitted. In addition, as an access system of the bi-directional bus, so called CSMA/CD (Carrier Sense Multiple Access with Collision Detection is employed in, e.g., D2B).

Communication from a sub-device included in a device to a sub-device included in any other device (hereinafter referred to as communication from sub-device to sub-device), communication from a sub-device included in a device to any other device (hereinafter referred to communication from sub-device to device), communication from a device to a sub-device included in any other device (hereinafter communication from device to sub-device), and communication from a device to any other device is carried out through the bi-directional bus.

The format of a transmit signal used in a bi-directional bus as described above, e.g., D2B will now be described. In D2B, control commands for controlling a sub-device of destination, etc. or data indicating the operating state, etc. are caused to have a frame configuration as shown in Fig. 1 of the accompanying drawings , and are transmitted through the bi-directional bus.

Namely, one frame consists of a header field 101 for specifying the header indicating the leading portion of the frame, a master address field 102 for specifying a source device address, a slave address field 103 for specifying a destination (receiving side) device address, a control field 104 for specifying control bits indicating communication, etc. in the state where a destination device is locked, or is not locked, and a data field 105 for specifying control commands or data.

The header of the header field 101 consists of, as shown in Fig. 2 of the accompanying drawings, a start bit 101a of one bit for providing synchronization, and mode bits 101b for prescribing a transmission speed (rate) or the number of bytes of the data field 105. These mode bits 101b are 1~3 bits. At present, three modes of mode 0 where the data field 105 is comprised of 2 bytes at the maximum, mode 1 where the data field 105 is comprised of 32 bytes at the maximum (16 bytes at the maximum in the case of communication from slave to master), and mode 2 where the data field 105 is comprised of 128 bytes at the maximum (64 bytes at the maximum in the case of communication from slave to master) are standardized.

The source device address of the master address field 102 consists of, as shown in the above-mentioned Fig. 2, master address bits 102a of 12 bits for specifying a source device address, and a parity bit 102b of 1 bit.

The destination device address of the slave address field 103 consists of, as shown in the above-mentioned Fig. 2, a slave address bits 103a of 12 bits for specifying a destination device address, a parity bit 103b of 1 bit, and an acknowledge bit 103c of 1 bit for responding from a destination device.

To the control field 104, as shown in the above-mentioned Fig. 2, control bits 104a of 4 bits indicating the direction of control commands or data, or indicating lock state or non-lock state, a parity bit 104b of 1 bit, and an acknowledge bit 104c of 1 bit are assigned.

In the data field 105, as shown in the above-mentioned Fig. 2, data bits 105a of 8 bits, end of data bit 105b of 1 bit parity bit 105c of 1 bit, and acknowledge bit 105d of 1 bit are repeated as occasion demands. Assuming now that data bits 105a are assumed to be data #1, #2, #3, ... in order from the beginning, in communication of, e.g., control commands, e.g., Operation code (hereinafter referred to as OPC) "Begin 2" (i.e., code "BD"h (h represents hexadecimal number)) indicating communication relating to sub-device, OPC "Begin 1" ("BC" h) indicating communication through HBS, and OPC "Begin 0" ("BB"h) indicating communication through other bus, etc. are assigned (allocated) to data #1. Further, e.g., in communication of data, data are assigned to data #1, #2 #3 ... every byte (8 bits).

OPR with respect to the above-described OPCs, e.g., OPR with respect to OPC "begin 2" consists of, as shown in Fig. 3, bits b_5, b_4, b_3, b_2 (b_7 is the Most Significant Bit (MSB) for identifying service codes of the Communication Telephony (CT) system, the Audio Video and Control (AV/C) system, and the Housekeeping (HK) system, etc.; and bits b_1, b_0 indicating any one of communication from sub-device to sub-device, communication from sub-device to device, communication from device to sub-device, and communication from device to device, viz., indicating presence or absence of Source Sub-Device Address (hereinafter referred to as SSDA) or Destination Sub-Device Address (hereinafter referred to as DSDA). It is to be noted that bit b_7 is caused to be always zero, and bit b_6 is reserved for future standardization and is caused to be 1 at present. In more practical sense, b_1=0, b_0=0 indicates communication from sub-device to sub-device; b_1=0, b_0=1 indicates communication from sub-device to device; b_1=1, b_0=0 indicates communication from device to sub-device; and b_1=1, b_0=1 indicates communication from device to device.

Now, in the case of transmitting data having a data quantity greater than a data capacity of the data field 105 in non-lock state from VTR to TV in a manner divided into 2 frames, for example, VTR constitutes, as shown in Fig. 4, two frames (so called a packet) P_1, P_2 in which master address bits are caused to be an address of VTR, slave address bits are caused to be an address of TV, control bits are caused to be a code (e.g., "F"h) indicating write of data in non-lock state, and data are assigned to data #1, #2, #3 ···. Then, VTR detects presence or absence of so called a carrier on the bi-directional bus to transmit frame P_1 when there is no carrier, i.e., the bi-directional bus is empty, thereafter to once stop sending of carrier to open the bi-directional bus. When the bi-directional bus is empty for a second time, VTR transmits frame P_2. Thus, transmission of data from VTR to TV is completed. The TV carries out display of characters based on this data.

In the case where VDP waits for the bi-directional bus to be open for transmitting data to the TV while the VTR is transmitting frame P_1, as shown in the above-mentioned Fig. 4, when the VTR transmitting frame P_1 thereafter stops sending the carrier, the VDP detects that there is no carrier on the bi-directional bus to acquire the right of use of the bi-directional bus to transmit, to the TV, a frame P3 in which master address bits, slave address bits, and control bits are respectively caused to be VDP address, the TV address and code "F"h (data/non-lock), and data are assigned to data #1, #2, #3 ···. At the time point when transmitting operation of VDP is completed, the VTR transmits frame P_2. Namely, since the VTR does not place the TV in a lock state, frame P_1 from the VTR, frame P_3 from VDP and frame P_2 from VTR are received in order by the TV. Since master address bits for identifying a source device are added to these frames, there is no possibility that an error in transmission, i.e., message (data) may be mixed. However, when data for display is sent from the VDP to the TV for a time period during which the VTR sends data to the TV to display status of the VTR on the screen of the TV, there is the possibility that there may take place an inconvenience such that display of the VDP breaks into display of VTR, or it takes too much time in the display of character, etc.

In view of this, in the bi-directional bus system, as shown in Fig. 5, a source device allows a destination (receiving side) device to be placed in a lock state to carry out transmission of data. Namely, as an example, the VTR transmits a frame P_1 in which master address bits are caused to take the address of the VTR, slave address bits are caused to take the address of the TV, control bits are caused to be code "A"h indicating write of control command in the lock state, and OPC "Begin 2", code "54"h indicating presence of SSDA and DSDA, address of, for example, a video deck, and address of, for example, the TV monitor code, code "EO"h indicating display, "20"h indicating, for example, the first line on the screen, code "22"h indicating, for example, the letter (character) of the standard size, and code "21"h indicating, for example, the small character of alphabet are respectively assigned to data #1 (OPC), data #2 (OPR), data #3 (SSDA), data #4 (DSDA), data #5 (OPC), data #6 (OPR1), data #7 (OPR2), and data #8 (OPR3), thus to carry out control to lock the TV. It is to be noted that SSDA and DSDA are assigned as occasional demands. For example, in communication from sub-device to device, DSDA is unnecessary. In communication from device to sub-device, SSDA is unnecessary. In communication from device to device, SSDA and DSDA are both unnecessary.

The, VTR transmits a frame P_2 in which master address bits, slave address bits, and control bits are caused to be respectively address of the VTR, address of the TV, and code "B"h indicating write of data in the lock state, and data of, e.g., 32 bytes at the maximum are assigned to data #1, #2, #3 ···. This operation is continued until a display line is changed.

Then, in order to give an instruction of line change, the VTR transmits a frame P_i in which master address bits, slave address bits, and control bits are caused to be respectively the address of the VTR, the address of the TV and the code "A"h (command/lock), and, in addition, code "EO"h, code "21"h indicating, for example, the second line on the screen, code "21"h indicating, for example, large letter (character), and code "20"h indicating, for example, capital of alphabet are respectively assigned to data #1 (OPC), data #2 (OPR1), data #3 (OPR2) and data #4 (OPR3) to subsequently transmit a frame P_{i+1} in which master address bits, slave address bits and control bits are caused to take respectively address of the VTR, ad-

dress of the TV and code "B"h (data/lock), and the remaining data are assigned to data #1, #2, #3 ···.

Thereafter, the VTR transmits a frame P_{j+2} in which master address bits, slave address bits and control bits are caused to take the address of the VTR, the address of the TV and code "E"h indicating write of control command in non-lock state, and end command (code "BE"h) indicating that a message (data communication) has been completed is assigned to data #1 (OPC) to release the lock of the TV.

In the case where, for example, the VTR completes transmission of frame P_2 so as to stop sending of the carrier when the data communication as described above is being carried out, when the VDP acquires the right of use of the bi-directional bus in order to transmit data to the TV to transmit a frame P_j in which master address bits, slave address bits and control bits are caused to take respectively the address of the VDP, the address of the TV and code "A"h (command/lock), and OPC "Begin 2", code "54"h, address of, for example, the video player, the address of, for example, the TV monitor, code "EO"h, code "20" (first line), code "22"h (standard letter (character)), and code "21"h (small letter (character) of alphabet) are respectively assigned to data #1 (OPC), data #2 (OPR), data #3 (SSDA), data #4 (DSDA), dat a #5 (OPC), data #6 (OPR1), data #7 (OPR2) and data #8 (OPR3), the TV informs that it is locked by the VDP. Thus, the VDP stops transmission of data. As a result, transmission of data from the VTR to the TV is continued without being interrupted by the VDP.

When transmission of data from the VTR to the TV is completed, as shown in the above-mentioned Fig. 5, the VDP transmits frame Pj to TV for a second time to place the TV in a lock state to subsequently transmit frame P_{j+1} in which master address bits, slave address bits and control bits are caused to take respectively the address of the VDP, address of the TV and code "B"h (data/lock), and data are assigned to data #1, #2, #3 ··· to subsequently transmit a frame P_{j+2} in which master address bits, slave address bits and control bits are caused to take respectively the address of the VDP, the address of the TV and the code "E"h (command/non-lock) and code "BE"h (end command) is assigned to data #1 (OPC) to release the lock of the TV.

Thus, data transmission from the VTR to the TV and data transmission from the VDP to the TV are completed. In accordance with such a transmission procedure, the bi-directional bus system solves the above-described problem that display of VDP breaks into display of VTR.

However, even in the case where a data quantity of data to be transmitted is less than the data capacity of the data field 105, and the data to be transmitted can be transmitted by one frame, the bi-directional bus system is adapted to place a destination (receiving side) device in a lock state thereafter to transmit data to release the lock of a device on the receiving side at the time point when transmission of data is completed.

Namely, as shown in Fig. 6, the VTR transmits a frame P_1 in which master address bits, slave address bits and control bits are caused to take respectively the address of the VTR, the address of the TV and the code "A"h (command/lock), and OPC "Begin 2", code "54"h, address of the video deck, address of the TV monitor, code "EO"h, code "20"h, code "22"h and code "21"h are respectively assigned to data #1 (OPC), data #2 (OPR), data #3 (SSDA), data #4 (DSDA), data #5 (OPC), data #6 (OPR1), data #7 (OPR2), and data #8 (OPR3) to control the TV so that it is placed in the lock state.

Then, the VTR transmits a frame P_2 in which the master address bits, slave address bits, and control bits are caused to take respectively the address of the VTR, the address of the TV and the code "B"h (data/lock), and data are assigned to data #1, #2, #3 ···.

Thereafter, the VTR transmits a frame P_3 in which the master address bits, slave address bits and control bits are caused to take respectively address of the VTR, address of the TV and code "E"h (command/lock), and code "BE"h (end command) indicating that message is completed is assigned to data #1 (OPC) to release the lock of the TV.

As stated above, in the communication method or bi-directional bus system, before actual data is transmitted, a frame for allowing a device on the receiving side to be placed in the lock state is required, and a frame for allowing the device on the receiving side to be placed in the non-lock state at the time point when transmission of data is completed is required, resulting in the problems that a traffic quantity is increased, the transmission efficiency is low, and the communication procedure (protocol) is complex, etc.

To achieve the above-mentioned object, a first transmitting method according to this invention is directed to a transmitting method for a bi-directional bus system in which a plurality of devices are connected to each other through a bi-directional bus,

wherein one frame of a transmit signal on the bi-directional bus consists of an address field for specifying addresses of devices between which communication is carried out, a control field for specifying whether communication is carried out in the state where a device on the receiving side is locked, or in the state where the device on the receiving side is not locked, and

a data field for specifying data to be transmitted, and wherein, in transmitting data to be transmitted having a data quantity of data greater than a data capacity of the data field in a manner divided into a plurality of frames,

the transmitting method comprises:

giving an indication to lock a device on the receiving side to the control field of a frame transmitted first;

giving an indication not to lock the device on the receiving side to the control field of a frame transmitted last; and

transmitting the transmit signal through the bi-directional bus.

Further, in transmitting, by one frame, data to be transmitted having a data quantity less than a data capacity of the data field by one frame,

the transmitting method may comprises:

giving an indication not to lock a device on the receiving side to the control field; and

Further, a receiving method according to this invention is directed to a receiving method for a bi-directional bus-system in which a plurality of devices are connected to each other through a bi-directional bus,

the receiving method comprising:

receiving, through the bi-directional bus, a transmit signal having a frame structure consisting of an address field for specifying address of devices between which communication is carried out, a control field for specifying whether a communication is carried out in the state where a device on the receiving side is locked or in the state where the device on the receiving side is not locked, and a data field for specifying data to be transmitted,

whereby when an indication to lock a device on the receiving side is given to the control field of a transmit signal from a first device, in the case where a transmit signal is received from a second device, the second device is informed through the bi-directional bus that the device on the receiving side is locked.

A communication method according to this invention is directed to a communication method for a bi-directional bus system in which a plurality of devices are connected to each other through a bi-directional bus,

a device on the transmitting side being adapted to transmit, through said bi-directional bus, a transmit signal in which one frame on the bi-directional bus consists of an address field for specifying addresses of devices between which communication is carried out, a control field for specifying whether a communication is carried out in the state where a device on the receiving side is locked or in the state where the device on the receiving side is not locked, and a data field for specifying data to be transmitted;

in transmitting data to be transmitted having a data quantity greater than a data capacity of the data field in a manner divided into a plurality of frames,

the device on the transmitting being operative to give an indication lock a device on the receiving side to the control field of a frame transmitted first, and to give an indication not to lock the device on the receiving side to the control field of a frame transmitted last, thus to transmit the transmit signal through the bi-directional bus,

a device on the receiving side being adapted to receive the transmit signal through the bi-directional bus,

whereby when the indication to lock the device on the receiving side is given to the data field of a transmit signal received from a first device on the transmitting side, in the case where a transmit signal is received from a second device on the transmitting side, the second device is informed through the bi-directional bus that the device on the receiving side is locked.

A first bi-directional bus system according to this invention comprises a plurality of devices and a bi-directional bus,

each of the plurality of device comprising:

transmit signal formation means for forming a transmit signal having a frame structure consisting of an address field for specifying addresses of devices between which communication is carried out, a control field for specifying whether a communication is carried out in the state where a device on the receiving side is locked or in the state where the device on the receiving side is not locked, and a data field for specifying data to be transmitted, whereby, in transmitting data to be transmitted having a data quantity greater than a data capacity of the data field, in a manner divided into a plurality frames, the transmit signal formation means is operative to give an indication to lock a device on the receiving side to the control field of a frame transmitted first, and to give an indication not to lock the device on the receiving side to the control field of a frame transmitted last, thus to transmit the transmit signal through the bi-directional bus; and

bus output means for outputting the transmit signal formed by the transmit signal formation means to the bi-directional bus,

the plurality of devices being connected to each other through the bi-directional bus.

Further, a second bi-directional bus system according to this invention comprises a plurality of devices and a bi-directional bus,

each of said plurality of devices comprising:

bus input means adapted to receive, through the bi-directional bus, a transmit signal having a frame structure consisting of an address field for specifying addresses of devices between which a communication is carried out, a control field for specifying whether a communication is carried out in the state where a device on the receiving side is locked or in the state where the device on the receiving side is not locked, and a data field for specifying data to be transmitted; and

control means adapted so that when an indication to lock a device on the receiving side is given to

the control field of a transmit signal from a first device received by the input means, in the case where a transmit signal is received from a second device, the second device is informed through the bi-directional bus that the device on the receiving side is locked,

the plurality of devices being connected to each other through said bi-directional bus.

In the bi-directional bus system each of the plurality of devices may further comprise:

bus input means adapted to receive the transmit signal through the bi-directional bus; and

control means adapted so that when the indication to lock the device on the receiving side is given to the control field of a transmit signal from a first device received by he bus input means, in the case where a transmit signal is received from a second device, the second device is informed that the device on the receiving side is locked,

the plurality of devices being connected to each other through the bi-directional bus.

Thus, in transmitting data to be transmitted having a data quantity greater than a data capacity of the data field in a manner divided into a plurality frames, an indication to lock a device on the receiving side is given at a frame transmitted first to the control field of a transmit signal consisting of address field, the control field, and data field, and an indication not to lock the device on the receiving side is given at a frame transmittee last to the control field of the transmit signal. The transmit signal thus indicated is transmitted through the bi-directional bus.

Also, in transmitting data to be transmitted having a data quantity less than data capacity of the data field by one frame, an indication not to lock device on the receiving side may be given to the control field of a transmit signal to transmit the transmit signal thus indicated through the bi-directional bus.

Thus, a transmit signal consisting of address field, control field and data field and such that an indication to carry out communication either in the state where a device on the receiving side is locked or in the state where the device on the receiving side is not locked is given to the control field may be received through the bi-directional bus. So that an indication to lock a device on the receiving side is given in the control field of a transmit signal from a first device, in the case where a transmit signal is received from a second device, the second device is informed through the bi-directional bus that the device on the receiving side is locked.

Devices on the transmitting side may be such that, in transmitting data to be transmitted having a data quantity greater than data capacity of the data field in a manner divided into a plurality of frames, the device is operative to give an indication to lock a device on the receiving side at a frame transmitted first to control field of a transmit signal consisting of address field, control field and data field and to give an indication not to lock the device on the receiving side at a frame transmitted last to the control field of the transmit signal to transmit the transmit signal through the bi-directional bus. On the other hand, devices on the receiving side receiving the transmit signal through the bi-directional bus, whereby when the indication to lock device on the receiving side is given to the control field of transmit signal received from a device on the transmitting side, in the case where a transmit signal is received from a second device on the transmitting side, the second device is informed through the bi-directional bus that the device on the receiving side is locked.

Further, each transmit signal formation means of a plurality of devices may be such that, in transmitting data to be transmitted having a data quantity greater than the capacity of the data field in a manner divided into a plurality of frames, the transmit signal formation means is operative to give an indication to lock device on the receiving side at a frame transmitted first to control field of a transmit signal consisting of address field, control field data field and to give an indication not to lock device on the receiving side of a frame transmitted last, thus to form transmit signal. The bus output means outputs this transmit signal to the bi-directional bus.

Also, each bus input means of a plurality of devices may receive, through bi-directional bus, a transmit signal consisting of address field, control field and data field and such that an indication to carry out communication either in the state where device on the receiving side is locked or in the state where device on the receiving side is not locked is given to the control field. Control means operate so that when indication to lock device on the receiving side is given to the control field of the received transmit signal from a first device, in the case where a transmit signal is received from a second device, the second device is informed that the device on the receiving side is locked.

Finally, each input means of a plurality of device may receive transmit signals through the bi-directional bus. Control means operates to that when indication to lock device on the receiving side is given to the control field of a transmit signal from a first device, in the case where a transmit signal is received from a second device, the second device is informed through the bi-directional bus that device on the receiving side is locked.

Thus, there may be provided a transmission method, a receiving method and a communication method for a bi-directional bus sytem, and a bi-directional bus system.

The present invention will be more clearly understood from the following description, given by way of example only, with reference to the accompanying drawings in which:

Fig. 1 is a view showing a conventional D2B

frame format.

Fig. 2 is a view showing the detail of the conventional D2B frame format.

Fig. 3 is a view for explaining OPR of OPC "Begin 2".

Fig. 4 is a view showing a conventional communication procedure (protocol) in non-lock state.

Fig. 5 is a view showing a conventional communication procedure (protocol) in lock-state.

Fig. 6 is a view showing a conventional communication procedure (protocol) when transmission is carried out by one frame in lock state.

Fig. 7 is a block diagram showing an actual configuration of a bi-directional bus system to which this invention is applied.

Fig. 8 is a block diagram showing an actual configuration of TV, VTR constituting the above-mentioned bi-directional bus system.

Fig. 9 is a view showing the structure of a connector of a bi-directional bus constituting the above-mentioned bi-directional bus system.

Fig. 10 is a view showing a frame format of a transmit signal for transmitting control command.

Fig. 11 is a view showing a format of a transmit signal for transmitting data.

Fig. 12 is a view showing a format of HDOPR of a transmit signal.

Fig. 13 is a view showing an actual example of a communication procedure when communication is carried out with data being divided into a plurality of frames.

Fig. 14 is a view showing an actual example of a communication procedure when data communication is carried out by one frame.

Fig. 15 is a flowchart for explaining the operation of a microprocessor of VTR constituting the bi-directional bus system.

A preferred embodiment of a transmitting method, a receiving method, and a communication method for a bi-directional bus system and a bi-directional bus system will now be described with reference to the attached drawings. In the embodiment, this invention is applied to D2B (Audio, Video and audiovisual systems Domestic Digital Bus) standardized by the publication 1030 of the so-called IEC, or a Home Bus System (hereinafter abbreviated as HBS) standardized by ET-2101 of EIAJ.

A bi-directional bus system to which this invention is applied has a configuration such that a television image receiver (hereinafter abbreviated as TV) 10 which is a device, video tape recorders (hereinafter each abbreviated as VDP) 20, 30 which are a device, and a video deck player (hereinafter abbreviated as VDP) 40 which is a device are connected to each other through a bi-directional bus 1, as shown in Fig. 7, for example.

The TV10 includes therein, as a sub-device, as shown in the above-mentioned Fig. 7, a tuner 10a adapted to receive a television (broadcasting) signal to reproduce a video signal and an audio signal therefrom, a TV monitor 10b for displaying a picture based on the video signal reproduced at the tuner 10a, and an amplifier 10c for amplifying the audio signal reproduced by the tuner 10a, and further comprises, as a sub-device, a switch box 10d for outputting to the external a video signal/audio signal (hereinafter referred to as an AV signal) from the tuner 10a, or delivering the AV signal inputted from the external to the tuner 10a and the TV monitor 10b.

Further, the VTR 20 includes as a sub-device therein, as shown in the above-mentioned Fig. 7, a video deck 20a adapted for recording an AV signal onto a magnetic tape, or reproducing the AV signal therefrom, and a tuner 20b adapted to receive a television (broadcasting) signal to reproduce an AV signal therefrom, and further comprises, as a sub-device, a switch box 20c adapted for outputting an AV signal from the video deck 20a or the tuner 20b to the external, or delivering an AV signal inputted from the external to the video deck 20a.

Further, the VTR30 includes therein, as a sub-device, a video deck 30a, a tuner 30b, and a switch box 30c similarly to the above-described VTR20.

In addition, the VDP 40 includes, as a sub-device, a video player 40a for reproducing an AV signal from an optical disk.

In this bi-directional bus system, e.g., video signals reproduced by VTR20, VTR30, VDP40 are delivered to the TV10 to display a picture based on this video signal on TV monitor 10b. In actual terms, the switch box 10d of the TV10 and the switch box 20c of the VTR20 are connected by an AV signal line L1, the switch box 10d of the TV10 and the switch box 30c of the VTR30 are connected by an AV signal line L2, and the switch box 10d of the TV10 and the video player 40a are connected by an AV signal line L3, viz., AV signal lines L1, L2, L3 are wired in a star form with the TV10 being as a center. Accordingly, AV signals reproduced by VTR20, VTR30, VDP40 are respectively delivered to the TV monitor 10b through AV signal lines L1, L2, L3 and switch box 10d. Thus, pictures corresponding thereto are displayed on the TV monitor 10b. Further, e.g., an AV signal reproduced by the video player 40a is delivered to video deck 20a through AV signal line L3, switch box 10d, AV signal line L1, and switch box 20c. Thus, they are recorded (image-recorded) onto a magnetic tape by video deck 20a.

Further, in this bi-directional bus system, e.g., the TV10 (device) controls, through the bi-directional bus 1, VTRs20, 30, VDP40 (devices) or video decks 20a, 30a, video player 40a, switch box 20c, 30c (sub-devices) included therein.

Further, in this bi-directional bus system, e.g., from VTRs 20. 30, VDP40, data indicating status, etc. thereof are delivered to TV10 through bi-directional

bus 1 in a manner divided into a plurality of frames (so called packet). TV10 displays, on TV monitor 10b, character, etc. based on these data.

In actual terms, the TV10 comprises, as shown in Fig. 8, for example, a microprocessor 12 for controlling the tuners 10a~ switch box 10d through internal control bus 11, a user interface unit 13 for inputting operation contents operated by user to the microprocessor 12, and a bus interface circuit 14 for inputting a transmit signal consisting of control commands for controlling other devices and sub-devices thereof or data indicating status, etc. from the bi-directional bus 1 and outputting it thereto.

Further, VTR20 comprises, as shown in the above-mentioned Fig. 8, a microprocessor 22 for controlling the video deck 20a~switch box 20c through an internal control bus 21, a user interface unit 23 for inputting operation contents operated by user to the microprocessor 22, and a bus interface circuit 24 for inputting a transmit signal from the bi-directional bus 1 or outputting it thereto. Further, VTR30, VDP40 similarly comprise a microprocessor and a bus interface circuit (not shown), etc.

In operation, when, e.g., user operates the user interface unit 13 of TV10 for the purpose of viewing, on TV10, a picture based on a video signal reproduced by VTR20, microprocessor 12 of TV10 forms a transmit signal in accordance with an operation content to transmit this transmit signal to the VTR20 through bus interface circuit 14 and the bi-directional bus 1. The microprocessor 22 of VTR20 carries out a control to play (reproduce) the video deck 20a through internal control bus 21 on the basis of the transmit signal received by bus interface circuit 24, and controls the switch box 20c so that an AV signal reproduced by the video deck 20a is delivered to TV10.

Namely, the user interface unit 13 comprises, as shown in the above-mentioned Fig. 8, an operation unit 13a provided with, e.g., a key switch, etc., and a display unit 13b provided with, e.g., a light emitting diode, etc. The operation unit 13a delivers a signal corresponding to an operation content that user has operated by using a key switch, etc. to microprocessor 12 through internal control bus 11.

The microprocessor 12 comprises, as shown in the above-mentioned Fig. 8, a Read Only Memory (hereinafter referred to as ROM) in which command Tables for converting received control commands to internal control commands for controlling the tuner 10a~switch box 10d or various programs such as a program for displaying a picture based on received data on TV monitor 10b, etc. are stored, a Central Processing Unit (hereinafter referred to as a CPU) for executing the program stored in the ROM12a, a Random Access Memory (hereinafter referred to as a RAM) 12c for storing result of the execution, or the like, and an I/O circuit 12d adapted to interface with the tuner 10a~bus interface circuit 14.

CPU 12b executes program stored in ROM12b to thereby generate a control command for controlling, e.g., VTR20 on the basis of a signal delivered through internal control bus 11, I/O circuit 12d from operation unit 13a to deliver this control command to bus-interface circuit 14 as a frame structure.

Further, CPU 12b delivers data such as status, etc. to bus interface circuit 14 as a frame structure, and carries out a control to display, e.g., status of VTR20 such as character, etc based on data received through bus interface circuit 14 on TV monitor 10b.

The bus interface circuit 14 employs, e.g., so called a CSMA/CD (Carrier Sense Multiple Access with Collision Detection) as an access system for the bi-directional bus 1 , and is connected to the bi-directional bus 1 through a connector standardized, e.g., by so called IEC/SC48B (Secretariat) 202.

In more practical sense, this connector is provided with, as shown in Fig. 9A, two sockets 2, 3. As shown in Fig. 9B, contacts 2a, 2b for signal, a contact 2c for earth of the socket 2, and contacts 3a, 3b for signal and contact 3c for earth of the socket 3 are connected to each other within the connector. Further, contacts 2a and 2b are connected through a switch 2d and a terminating resistor (e.g., 120m ohm) 4, and contacts 3a and 3b are connected through a switch 3d and the terminating resistor 4.

Connectors constructed in this way are respectively provided every respective devices such as TV10, etc. Like connectors provided in the VTR20, for example, when a plug of the bi-directional bus 1 from the TV10 and a plug of the bi-directional bus 1 from the VTR30 are respectively inserted into sockets 2, 3, the switches 2d, 3d are opened so that the terminating resistor 4 is cut off. As a result, a transmit signal from TV10 is delivered to the bus interface circuit 24 of VTR20, and is delivered to VTR30 or VDP40 of the succeeding stage.

The format of a transmit signal transmitted on the bi-directional bus 1 will now be described. The format of this transmit signal is substantially in conformity with the format of D2B described in the prior art, and control commands or data for controlling a destination sub-device, etc. or data for displaying on TV10 status, etc. are caused to have a frame structure as shown in Figs. 10, 11. Thus, control commands or data of such frame structure are transmitted.

Namely, one frame consists of a header field 51 for specifying the header indicating the leading portion of the frame, a master address field 52 for specifying a source device address, a slave address field 53 for specifying a destination device address, a control field 54 for specifying a control bit indicating a communication, etc. in the state where destination device is locked, or in the state where the destination device is not locked, and a data field 55 for specifying control commands or data.

The header of the header field 51 is in conformity with the D2B described in the prior art (see Fig. 2), and consists of a start bit of 1 bit for providing synchronization, and mode bits for prescribing a transmission speed or the number of bytes of the data field 55.

The source device address of the master address field 52 is in conformity with the D2B described in the prior art, and consists of master address bits of 12 bits for specifying a source device address, and a parity bit of 1 bit.

The destination device address of the slave address field 53 is in conformity with the D2B described in the prior art, and consists of slave address bits of 12 bits for specifying a destination device address, and an acknowledge bit of one bit for responding acknowledge from the destination device.

To the control field 54, substantially in conformity with the D2B described in the prior art, control bits of 4 bits for specifying whether the data field 55 is control command or data, a parity bit of 1 bit, and an acknowledge bit of 1 bit are assigned. It is to be noted that as the control bit, there are used only code "E"h (h indicates hexadecimal number) indicating write in non-lock state of control command, code "B"h indicating write in lock state of data, and code "F"h indicating write in non-lock state of data, which are codes from master to slave of codes standardized in D2B.

In the data field 55, data bits of 8 bits, end of data bit of 1 bit, parity bit of 1 bit, and acknowledge bit of 1 bit are repeated as occasion demands substantially in conformity with the D2B described in the prior art. When data bits are assumed to be data #1, #2, #3 ··· from the beginning in order, a route select code indicating a communication from a sub-device included in a device to any other device, a communication from a device to a sub-device included in any other device, or a communication from a device to any other device is assigned to data #1 ~data #3 as shown in the above-mentioned Figs. 10, 11.

This route select code consists of, as shown in the above-described Figs. 10, 11, a text header of 8 bits, a header operand comprised of 8 bits indicating communication from sub-device included in device to any other device, communication from device to sub-device included in any other device, or communication from device to any other device, and a sub-device address comprised of 8 bits indicating a Source Sub-Device Address (hereinafter referred to as SSDA) or Destination Sub-device Address (hereinafter referred to as DSDA). The text header is assigned to data #1 as "AB"h to discriminate from OPC "Begin 2" (code "BD"h), OPC "Begin 1" ("BC"h), OPC "Begin 0" ("BB"h) used in the conventional D2B.

The header operand (hereinafter referred to as HDOPR) subsequent to the text header is assigned to data #2. For example, as shown in Fig. 12, by bits b_1, b_0 of the lower order 2 bits (b_7 is the most significant bit (MSB)), communication from sub-device included in device to any other device (hereinafter referred to as communication from sub-device to device), communication from device to sub-device included in any other device (hereinafter referred to as communication from device to sub-device), or communication from device to any other device is designated. In more practical sense, b_1=0, b_0=1 indicates communication from sub-device to device, b_1=1, b_0=0 indicates communication from device to sub-device, and b_1=1, b_0=1 indicates communication from device to device. Namely, in this bi-directional bus system, communication from a sub-device included in a device to a sub-device included in any other device used in the conventional D2B is not carried out. In other words, HDOPR where b_1=0 and b_0=0 is not used.

In communication of control commands, as shown in the above-mentioned Fig. 10, control commands, etc. are assigned to data #4 and data subsequent thereto. On the other hand, in communication of data, as shown in the above-mentioned Fig. 11, Data Attribute (hereinafter referred to as DTATR) for identifying, e.g., so called ASCII code, On Screen Data (hereinafter referred to as OSD) for displaying character, etc. on TV monitor, Japanese OSD data, transparent transfer data for transferring an instruction, e.g., from a received remocon to other device as it is, or the like is assigned to data #4, the number of bytes of data (hereinafter referred to as BYTE) included in that frame is assigned to data #5 by codes "20"h~"2F"h respectively corresponding to, e.g., 1 byte~16 bytes, and data are assigned to data #6 and data subsequent thereto every byte.

Meanwhile, in communication of data, when data capacity of data field 55, e.g., data capacity prescribed by mode bits of the above-described header field 51 is, e.g., 16 bytes and a quantity of data transmitted is more than that, transmit data is transmitted in a manner divided into a plurality of frames, and control bits of the above-described control field 54 of a frame to be transmitted first are designated so that a device on the receiving side is locked, i.e., are set to code "B"h indicating write in lock state of data, and control bits transmitted last are designated so that device on the receiving side is not locked, i.e., is set to code "F"h indicating write in non-lock state of data. It is to be noted that when a data quantity of data transmitted is less than data capacity of the data field 55, and data to be transmitted is transmitted by one frame, control bits are caused to indicate that a device on the receiving side is not locked, i.e., are set to code "F"h indicating write in non-lock state of data.

Accordingly, in carrying out communication of control commands, e.g., sending a control command for playing, e.g., video deck 20a from TV10 (device) to video deck 20a (sub-device) included in VTR20 (other device), microprocessor 12 of TV10 assigns an address of TV10 as master address bits to the master

address field 52, assigns an address of VTR20 as slave address bits to the slave address field 53, and assigns code "E"h indicating write of the control command from master to slave to the control field 54 as control bits. Further, the microprocessor 12 assigns code "AB"h as a text header to data #1, assigns a code (b_1=1, b_0=0) indicating communication from device to sub-device to data #2 as HDOPR, and assigns an address of video deck 20a to data #3 as DSDA. Further, the microprocessor 12 assigns code "C3"h for playing, e.g., the video deck to data #4 subsequent thereto as OPC, and assigns code "75"h indicating forward to data #5 as OPR.

In addition, in transmitting, e.g., from TV (device) to VTR20 (device), a control command to turn OFF power supply, microprocessor 12 assigns code (b_1=1, b_0=1) indicating communication from device to device to data #2 as HDOPR. In this case, since an address of the sub-device is unnecessary, microprocessor 12 assigns a dummy code, e.g., code "7F"h to data #3. Further, the microprocessor 12 assigns, e.g., code "AO"h indicating standby to data #4 as OPC, and assigns code "70"h indicating ON to data #5 as OPR.

On the other hand, in carrying out communication of data, e.g., in transmitting data indicating status, etc. of video deck 20a (sub-device) from VTR20 to TV10 in a manner divided into a plurality of frames, e.g., two frames P_1, P_2 to display a picture based on those data on TV10, microprocessor 22 of VTR 20 assigns, as shown in Fig. 13, for example, address of VTR20 to the master address field 52 as master address bits, assigns address of TV10 to the slave address field 53 as slave address bits, and assigns code "B"h indicating write in lock state of data from master to slave to the control field 54 as control bits.

Further, the microprocessor 22 assigns code "AB"h to data #1 as text header, assigns code (b_1=0, b_0=1) indicating communication from sub-device to device to data #2 as HDOPR, and assigns address of video deck 20a to data #3 as SSDA.

Further, microprocessor 22 assigns code "20"h indicating, e.g., OSD data to data #4 as DTATR, and assign code "2A"h indicating e.g., that data of one byte is included in this frame to data #5 as BYTE.

Further, microprocessor 22 assigns code "20"h indicating, e.g., first line on screen to data #6 as OPR1, assigns code "22"h , e.g., indicating a character of the standard size to data #7 as OPR2, and assigns code "21"h indicating, e.g., small letter (character) of alphabet to data #8 as OPR3.

Then, microprocessor 22 assigns data to be transmitted to data #9~data #16 every byte. Thus, a frame P_1 transmitted first is formed.

At a frame P_2 transmitted last, as shown in the above-mentioned Fig. 13, microprocessor 22 assigns address of VTR20 to master address field 52 as master address bits, assigns address of TV10 to slave address field 53 as slave address bits, and assigns code "F"h indicating write in non-lock state of data from master to slave to control field 54 as control bits.

Further, microprocessor 22 assigns code "AB"h to data #1 as text header, assigns code (b_1=0, b_0=1) indicating communication from sub-device to device to data #2 as HDOPR, and assigns address of video deck 20a to data #3 as SSDA.

In addition, microprocessor 22 assigns code "20"h indicating, e.g., OSD data to data #4 as DTATR, and assigns code "27"h indicating that data of 8 bytes are included in this frame to data #5 as BYTE.

Meanwhile, when, e.g., display condition on screen is not changed, i.e., character of the same size, etc. is displayed on the same line, the above-described OPR1~OPR3 become unnecessary. Microprocessor 22 assigns data to be transmitted to data #6~data #13 every bytes. Thus, as shown in the above-mentioned Fig. 13, a frame P_2 transmitted last is formed.

In communication of data in which a data quantity of data to be transmitted is less and data indicating status, etc. of video deck 20a is transmitted, e.g., from VTR20 to TV10 by one frame P_1, as shown in Fig. 14, for example, microprocessor 22 of VTR20 assigns address of VTR20 to master address field 52 as master address bits, assigns address of TV10 to slave address field 53 as slave address bits, and assigns code "F"h indicating write in non-lock state of data from master to slave to control field 54 as control bits.

Further, microprocessor 22 assigns code "AB"h to data #1 as text header, assigns code (b_1 = 0, b_0 = 1) indicating communication from sub-device to device to data #2 as HDOPR, and assigns address of video deck 20a to data #3 as SSDA.

Further, microprocessor 22 assigns code "20"h indicating, e.g., OSD data to data #4 as DTATR, assigns code "2A"h indicating that byte of 11 bytes are included in this frame to data #5 as BYTE.

Further, microprocessor 22 assigns code "20"h indicating, e.g., first line on screen to data #6 as OPR1, assigns code "21"h indicating, e.g., large letter (character) to data #7 as OPR2, and assigns code "20"h indicating, e.g., capital of alphabet to data #8 as OPR3.

Then, microprocessor 22 assigns data to be transmitted to data #9~data~#16 every byte. Thus, a frame P_1 when data is transmitted by one frame is formed.

Namely, when it is assumed that data quantity of data to be transmitted is X, and a data capacity which can be transmitted by one frame is n, microprocessor 22 forms a frame in accordance with the flowchart shown in Fig. 15.

At step ST1, microprocessor 22 judges whether or not data quantity X is greater than data capacity n. As a result, if so, the operation proceeds to step ST2.

If not so, the operation proceeds to step ST5.

At step ST2, microprocessor 22 places control bits in lock state to form a frame. Then, the operation proceeds to step ST3.

At the step ST3, microprocessor 22 sends the frame formed at the step ST2. Then, the operation proceeds to step ST4.

At step ST4, data capacity n in subtracted from data quantity X to allows that value obtain by subtraction to be newly data quantity X, i.e., calculate the remaining data quantity X. Then, the operation returns to the step ST1.

On the other hand, at step ST5, microprocessor 22 places control bits in non-lock state to form a frame. Then, the operation proceeds to step ST6.

At the step ST6, microprocessor 22 sends the frame formed at the step ST5. The operation is completed. In transmitting data in a manner divided into a plurality of frames, microprocessor 22 carries out of formation of a frame such that frames from a frame transmitted first to a frame earlier by one than a frame transmitted last are caused to be in lock state and the frame transmitted last is caused to be in non-lock state. Further, in transmitting data by one frame, microprocessor 22 forms a frame in which that frame is caused to be in non-lock state.

As stated above, in this bi-directional bus system, a frame allowing a destination (receiving side) device to be in lock state before actual data is transmitted and a frame allowing data on the receiving side to be placed in non-lock state at the time point when transmission of data is completed, which were required in the conventional bi-directional bus system, are unnecessary. Accordingly, the traffic quantity can be reduced to much more degree as compared to the conventional system. Thus, the transmission efficiency can be improved. In addition, the communication procedure can be simplified.

A transmit signal having frame structure as described above is delivered from the microprocessor 12 of TV 10 to interface circuit 14, or delivered from microprocessor 22 of VTR20 to bus interface circuit 24. These bus interface circuits 14, 24 detect presence or absence of so called a carrier on the bi-directional bus 1 to transmit the transmit signal to TV10, VTR20, 30 and VDP40, etc. through the bi-directional bus 1 when there is no carrier, i.e., the bi-directional bus 1 is empty.

In transmission of control command from TV10 to VTR20, for example, bus interface circuit 24 of VTR20 receive transmit signal trough bi-directional bus 1, and delivers the received transmit signal to microprocessor 22. The microprocessor 22 executes program (software) stored in, e.g., ROM 22a to detect, from the transmit signal, the route select code inserted at a predetermined position of the data field 55 to detect on the basis of the detected route select code whether communication carried out is communication from sub-device included in device to any other device, communication from device to sub-device included in any other device, or communication from device to any other device.

In actual terms, microprocessor 22 detects, on the basis of master address bits of the master address field 52 and slave address bits of the slave address field 53 of the transmit signal, that this transmit signal is a transmit signal for the microprocessor 22 from, e.g., TV10, and detects, on the basis of the code of the control field 54, write of control command from master to slave by, e.g., code "E"h. It is to be noted that microprocessors of VTR30 and VDP40 detect that a current communication is not a communication for VTR or VDP from the fact that the slave address bits do not corresponds to their own addresses, thus not to carry out the operation corresponding to that transmit signal.

Further, microprocessor 22 detects, on the basis of the text header assigned to data #1 of the data field 55, that a current code is not OPC "Begin 2" (code "BD"h), OPC "Begin 1" ("BC"h), or OPC "Begin 0" ("BB"h) used in the conventional D2B by, e.g., code "AB"h, and detects the kind of communications on the basis of HDOPR assigned to data #2, i.e., when, e.g., the lower order 2 bits are 1, 0 (b_1=1, b_0=0), microprocessor 22 detects that a current communication is communication from device to sub-device; when those bits are b_1=0, b_0=1, it detects that current communication is communication from sub-device to device, and when those bits are b_1=1, b_0=1, it detects that current communication is communication from device to device. Namely, even if a transmit signal in conformity with the conventional D2B is transmitted through the same bi-directional bus 1, discrimination therebetween can be made.

At the time of communication from device to sub-device, microprocessor 22 recognizes that DSDA is assigned to data #3. At the time of communication from sub-device to device, microprocessor 22 recognizes that SSDA is assigned to data #3. Further, at the time of communication from device to device, the microprocessor 22 recognizes that data #3 is dummy code "7F"h. In addition, microprocessor 22 specifies, on the basis of DSDA assigned to, e.g., data #3, that a current control is, e.g., control for video deck 20a.

Meanwhile, respective equipments (devices) such as VTR20, etc. have a command Table for converting control commands to internal control commands for controlling sub-devices every sub-devices that those devices include therein, thus to convert (decode) the same control command to internal control command of control contents corresponding to various controlled system sub-devices. In more practical sense, in ROM 22a of the microprocessor 22, for example, a deck/player command Table for video deck 20a, and a tuner command Table for tuner 20b are stored. The microprocessor 22 decodes control

commands assigned to data #4, #5 of the data field 55 into internal control commands for controlling the video deck 20a ~ switch box 20c on the basis of these command Tables to control the video deck 20a ~ switch box 20c through the internal control bus 21 on the basis of the internal control commands. Namely, e.g., in OPC of the control commands, code "C0"h indicates a repeat in the deck/player command, indicates control of the band in the tuner command, indicates control of contrast in the video command, and indicates control of volume in the audio command. In other words, a command Table determined by a default value of a sub-device specified by DSDA is used. As a result, code of the same control command can be commonly used so as to cope with various sub-devices. Thus, the control command can be shortened.

For example, when DSDA is video deck 20a, OPC of the control command is code "C3"h, and OPR is code "75"h, microprocessor 22 of VTR20 decodes a control command into an internal control command indicating play and forward by using the deck/player command Table to carry out a control so that the video deck 20a conducts a reproducing operation through the internal control bus 21, and to carry out a control so that an AV signal from the video deck 20a is delivered to the switch box 10d of TV10 through switch box 20c. In this way, communication from TV10 (device) to video deck 20a (sub-device) of VTR20 is carried out. Thus, user can view, on TV10, a picture based on the AV signal reproduced by the VTR20.

On the other hand, in transmitting data indicating status of video deck 20a, e.g., from VTR20 to TV10 described above, bus interface circuit 14 of TV10 receives a transmit signal through bi-directional bus 1, and delivers the received transmit signal to microprocessor 12. The microprocessor 12 executes program (software) stored in ROM 12a to detect a route select code inserted at a predetermined position of data field 55 from the transmit signal to detect on the basis of the detected route select code whether a current communication is communication from a sub-device included in a device to any other device, communication from a device to a sub-device included in any other device, or communication from a device to any other device.

In actual terms, microprocessor 12 detects on the basis of master address bits of the master address field 52 and slave address bits of the slave address field 53 of a transmit signal, that this transmit signal is, e.g., a transmit signal for microprocessor 12 from VTR20, and detects on the basis of the code of the control field 54 that a write operation is writing in a lock state of data when corresponding code is, e.g., code "B"h and that a write operation is writing in non-lock state of data when corresponding code is code "F"h. Namely, when data is transmitted in a manner divided into a plurality of frames, microprocessor 12 detects that a current write operation is a write operation in lock state of data from the first frame and write operation in non-lock state of data at the last frame. Further, when data is transmitted in the state of one frame, microprocessor 12 detects that a current write operation is a write operation in non-lock state of data at that frame. When microprocessor 12 receives the first frame of a transmit signal delivered from a first device, e.g., VTR20, it is placed in lock state. When microprocessor 12 receives a transmit signal from a second device, e.g., VDP40, it neglects that received signal (allows that received signal to be invalid), and informs VDP40 that corresponding device is in lock state (locked) as described later.

Further, microprocessor 12 detects on the basis of text header assigned to data #1 of data field 55 that a current code is not OPC "Begin 2" (code "BD"h), OPC "Begin 1" ("BC"h), OPC "Begin 0" ("BB"h), and detects on the basis of HDOPR assigned to data #2, that when the lower order two bits are 1, 0 (b_1=1, b_0=0), a current communication is communication from device to sub-device, that when those bits are b_1=0, b_0=1, a current communication is communication from sub-device to device, that when those bits are b_1=1, b_0=1, a current communication is communication from device to device.

Further, microprocessor 12 recognizes that DSDA is assigned to data #3 when a current communication is communication from device to sub-device, that SSDA is assigned to data #3 when a current communication is communication from sub-device to device, and that data #3 is dummy code "7F"h when a current communication is communication from device to device. Further, microprocessor 12 specifies current data as data from, e.g., video deck 20a on the basis of SSDA assigned to data #3, for example.

Further, microprocessor 12 discriminates the kind of data assigned to data #9 ~ data #16, for example, on the basis of DTATR assigned to data #4. In more practical sense, microprocessor 12 recognizes that when a current code is, e.g., code "20"h, received data is ASCII code, OSD data, that when a current code is, e.g., code "21"h, received data is Japanese OSD data, and that when a current code is, e.g., code "22"h, received data is transparent transmit data.

Further, microprocessor 12 detects the number of bytes of data transmitted at this frame on the basis of BYTE assigned to data #5. In more practical sense, microprocessor 12 detects 1 ~ byte 16 bytes respectively in correspondence with codes "20"h ~ "2F"h, for example. Namely, microprocessor 12 can recognize in advance data quantity of data included in frame, thus making it possible to simplify processing (software) for judging the end of that frame.

Further, microprocessor 12 detects on the basis of OPR1 assigned to data #6 on which line of TV monitor 10b display is carried out. In more practical sense, microprocessor 12 detects the first line, the second

line, the third line ··· respectively in correspondence with codes "20"h, "21"h, "22"h ···.

Further, microprocessor 12 detects the size of a character displayed on TV monitor 10b on the basis of OPR2 assigned to data #7. In more practical sense, microprocessor 12 detects that when a current code is code "20"h, a character displayed is a character of the standard size, and that when a current code is code "21"h, a character displayed is a large letter (character).

Further, microprocessor 12 detects capital or small letter (character) of alphabet on the basis of OPR3 assigned to data #8. In more practical sense, microprocessor 12 detects that when a current code is, e.g., code "20"h, a corresponding character is large letter (character), and when a current code is, e.g., code "21"h, a corresponding character is a small letter (character). It is to be noted that when data is divided into a plurality of frames and display condition on screen is not changed, i.e., a character of the same size, etc. is displayed on the same line, these OPR1 ~ OPR3 are received only at the first frame, and are not received at the subsequent frames.

Further, microprocessor 12 carries out a control to display, under the condition designated by the above-described OPR1~OPR3, characters, etc. based on data assigned to data #9~data #16 on TV monitor 10b. Thus, communication of data indicating status, etc. from video deck 20a (sub-device) of VTR20 to TV10 is carried out. One can view the operating state of, e.g., VTR20 on TV10.

Meanwhile, in the case where VDP 40 waits that the bi-directional bus 1 is opened in order to transmit data to TV10 for a time period during which VTR20 is transmitting frame P_1, if VTR has transmitted frame P_1 thereafter to stop sending of carrier, VDP40 detects there is no carrier on the bi-directional bus 1 to acquire the right of use of the bi-directional bus 1 to transmit, as shown in Fig. 13, to TV10, frame P_3 in which master address bits, slave address bits and control bits are caused to be respectively address of VDP40, address of TV10, code "F"h (data/non-lock); and code "AB"h, code indicating communication from sub-device to device, address of video player, code "20"h (OSD data), code "2A"h (11 bytes), code "20"h (first line), code "22"h (standard character), and code "21"h (small letter (character) of alphabet) are respectively assigned to data #1 (text header), data #2 (HDOPR), data #3 (SSDA), data #4 (DATAR), data #5 (BYTE), data #6 (OPR1), data #7 (OPR2); and data #8 (OPR3), and data are assigned to data #9~data #16.

Microprocessor 12 receives this frame P_3, but detects on the basis of slave address bits (address of VDP40) that frame P_3 is not a frame from VTR20, and disregards frame P_3. Since microprocessor 12 is locked because it receives frame P_1 from VTR20, it informs VDP40 that it is locked. In more actual sense, microprocessor 12 sends back acknowledge with respect to control bits of frame P_3 received from VDP40 as so called NACK indicating failure to reception. Then, VDP40 stops transmission of data by NACK. As a result, microprocessor 12 can receive data from VTR20 without being interrupted.

When transmission of data from VTR20 to TV10 is completed, i.e., after frame P_2 placing TV10 in non-lock state is transmitted as shown in the above-mentioned Fig. 13, VDP40 transmits frame P_3 to TV10 for a second time.

On the other hand, when a data quantity of data transmitted is less and VTR20 is transmitting data by one frame as shown in the above-mentioned Fig. 14, VTR20 is placed in non-lock state as described above. Accordingly, when transmission of frame P_1 from VTR20 is completed and the bi-directional bus becomes empty, VDP40 can immediately transmit frame P_2.

It is to be noted that this invention is not limited to the above-described embodiment, but can be applied to, e.g., a communication to send a request from a device to a sub-device to send an answer from sub-device back to device, e.g., a communication for automatically informing the status of device, or the like. In addition, it is needless to say that this invention can be applied to, e.g., a bi-directional bus system adapted to control AV equipment, etc. except for D2B or HBS.

As apparent from the foregoing description, in accordance with this invention, in transmitting data to be transmitted having a data quantity greater than data capacity of the data field in a manner divided into a plurality of frames, the transmitting method comprises: giving an indication to lock a device on the receiving side at a frame transmitted first to control field of a transmit signal consisting of address field, the control field and data field; giving an indication not to lock the device on the receiving side at a frame transmitted last to control field of the transmit signal; and transmitting the transmit signal through the bi-directional bus. As a result, a frame placing a device on the receiving side in a lock state before actual data is transmitted and a frame placing a device on the receiving side in non-lock state at the time point when transmission of data is completed, which were required in the conventional bi-directional bus system, are unnecessary. Accordingly, the traffic quantity can be reduced to much more degree as compared to the conventional system. Thus, the transmission efficiency can be improved. In addition, the communication procedure can be simplified.

Further, in this invention, in transmitting data to be transmitted less than data capacity of data field by one frame, the transmitting method comprises: giving an indication not to lock a device on the receiving side to the control field of a transmit signal; and transmitting the transmit signal through the bi-directional

bus. As a result, a frame placing a device on the receiving side in a lock state before actual data is transmitted and a frame placing a device on the receiving side in non-lock state at the time point when transmission of data is completed, which were required in the conventional bi-directional bus system, are unnecessary. Accordingly, the traffic quantity can be reduced to much more degree as compared to the conventional system. Thus, the transmission efficiency can be improved. In addition, the communication procedure can be simplified.

In addition, in this invention, the communication method comprises: receiving, though bi-directional bus, a transmit signal consisting of address field, control field and data field, and such that an indication to carry out communication either in state where device on the receiving side is locked or in the state where device on the receiving side is not locked is given to the control field, whereby when indication to lock device on the receiving side is given to the control field of a transmit signal from a first device, in the case where a transmit signal is received from a second device, the second device is informed through the bi-directional bus that the device on the receiving side is locked. As a result, the second device stops transmission of a transmit signal, thus making it possible to receive the transmit signal from the first device without being interrupted.

Claims

1. A transmitting method for a bi-directional bus system in which a plurality of devices are connected to each other through a bi-directional bus, wherein one frame of a transmit signal on the bi-directional bus comprises an address field for specifying addresses of devices between which communication is to be carried out, a control field for specifying whether communication is to be carried out in the state where a device on the receiving side is locked, or in the state where the device on the receiving side is not locked, and a data field for specifying data to be transmitted, the transmitting method comprising:

   transmitting the transmit signal through said bi-directional bus; and

   where transmitting date having a data quantity greater than the data capacity of a data field in a manner divided into a plurality of frames,

   providing in the control field of a frame transmitted first an indication to lock a device on the receiving side, and

   providing in the control field of a frame transmitted last an indication to unlock/not to lock the device on the receiving side.

2. A transmitting method as set forth in claim 1, the transmitting method comprising, where transmitting data having a data quantity less than a data capacity of the data field in one frame, providing in the control field an indication not to lock a device on the receiving side.

3. A receiving method for a bi-directional bus-system in which a plurality of devices are connected to each other through a bi-directional bus,

   the receiving method comprising:

   receiving, through said bi-directional bus, a transmit signal having a frame structure comprising of an address field for specifying addresses of devices between which communication is to be carried out, a control field for specifying whether communication is to be carried out in the state where a device on the receiving side is locked or in the state where the device on the receiving side is not locked, and a data field for specifying data to be transmitted,

   whereby when an indication to lock a device on the receiving side is provided in the control field of a transmit signal from a first device, in the case where a transmit signal is received from a second device, said second device is informed through said bi-directional bus that the device on the receiving side is locked.

4. A communication method comprising a transmitting method according to claim 1 or 2 and a receiving method according to claim 3.

5. A communication method for a bi-directional bus system in which a plurality of devices are connected to each other through a bi-directional bus,

   a device on the transmitting side being adapted to transmit, through said bi-directional bus, a transmit signal in which one frame on the bi-directional bus comprises an address field for specifying addresses of devices between which communication is to be carried out, a control field for specifying whether communication is to be carried out in the state where a device on the receiving side is locked or in the state where the device on the receiving side is not locked, and a data field for specifying data to be transmitted,

   where transmitting data having a data quantity greater than a data capacity of the data field in a manner divided into a plurality of frames, the device on the transmitting side being arranged to give an indication in the control field of a frame transmitted first to lock a device on the receiving side and to give an indication in the control field of a frame transmitted last to unlock/not to lock the device on the receiving side, thus to transmit the transmit signal through said bi-directional bus,

   a device on the receiving side being adapt-

ed to receive a transmit signal through said bi-directional bus,

whereby when the indication to lock the device on the receiving side is given in the data field of a transmit signal received from a first device on the transmitting side, in the case where a transmit signal is received from a second device on the transmitting side, said second device is informed through said bi-directional bus that the device on the receiving side is locked.

6. A bi-directional bus system comprising a plurality of devices and a bi-directional bus,

each of said plurality of device comprising:

transmit signal formation means for forming a transmit signal having a frame structure comprising of an address field for specifying addresses of devices between which communication is to be carried out, a control field for specifying whether communication is to be carried out in the state where a device on the receiving side is locked or in the state where the device on the receiving side is not locked, and a data field for specifying data to be transmitted, whereby, for transmitting data having a data quantity greater than a data capacity of the data field in a manner divided into a plurality frames, said transmit signal formation means being arranged to give an indication in the control field of a frame transmitted first to lock a device on the receiving side and to give an indication in the control field of a frame transmitted last unlock/not to lock the device on the receiving side, thus to form the transmit signal; and

bus output means for outputting the transmit signal formed by said transmit signal formation means to said bi-directional bus,

said plurality of devices being connected to each other through said bi-directional bus.

7. A bi-directional bus system comprising a plurality of devices and a bi-directional bus,

each of said plurality of devices comprising:

bus input means adapted to receive, through said bi-directional bus, a transmit signal having a frame structure comprising an address field for specifying addresses of devices between which communication is to be carried out, a control field for specifying whether communication is to be carried out in the state where a device on the receiving side is locked or in the state where the device on the receiving side is not locked, and a data field for specifying data to be transmitted; and

control means adapted so that when an indication to lock a device on the receiving side is given in the control field of a transmit signal from a first device received by said bus input means, in the case where a transmit signal is received from a second device, said second device is informed through said bi-directional bus that the device on the receiving side is locked,

said plurality of devices being connected to each other through said bi-directional bus.

8. A bi-directional bus system according to claim 6 wherein each of said plurality of devices further comprises:

bus input means adapted to receive the transmit signal through said bi-directional bus; and

control means adapted so that when the indication to lock a device on the receiving side is given to the control field of a transmit signal from a first device received by said bus input means, in the case where a transmit signal is received from a second device, the second device is informed that the device on the receiving side is locked,

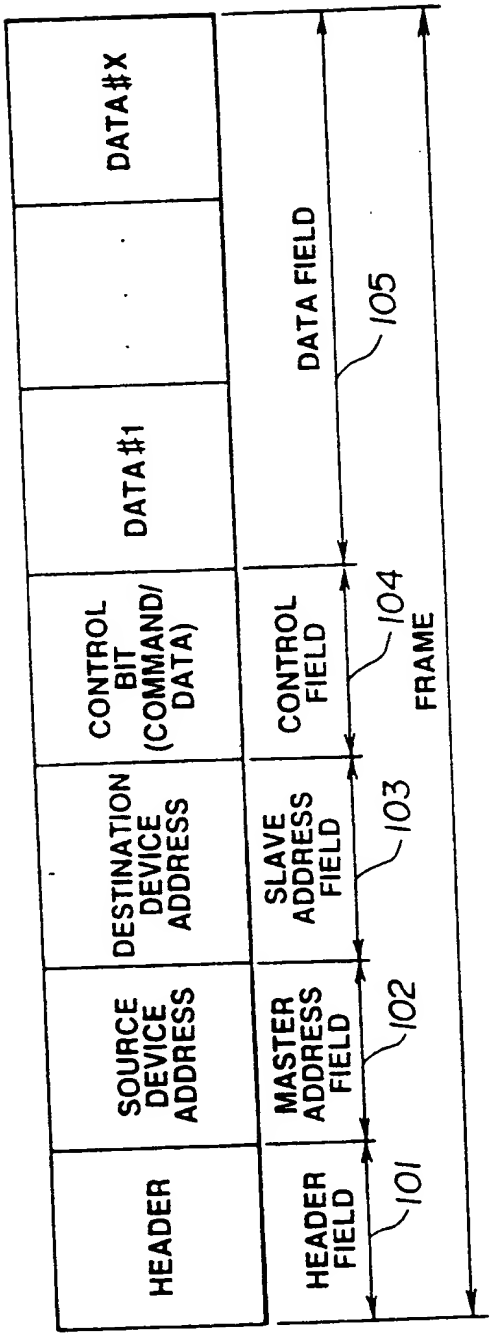


FIG.1

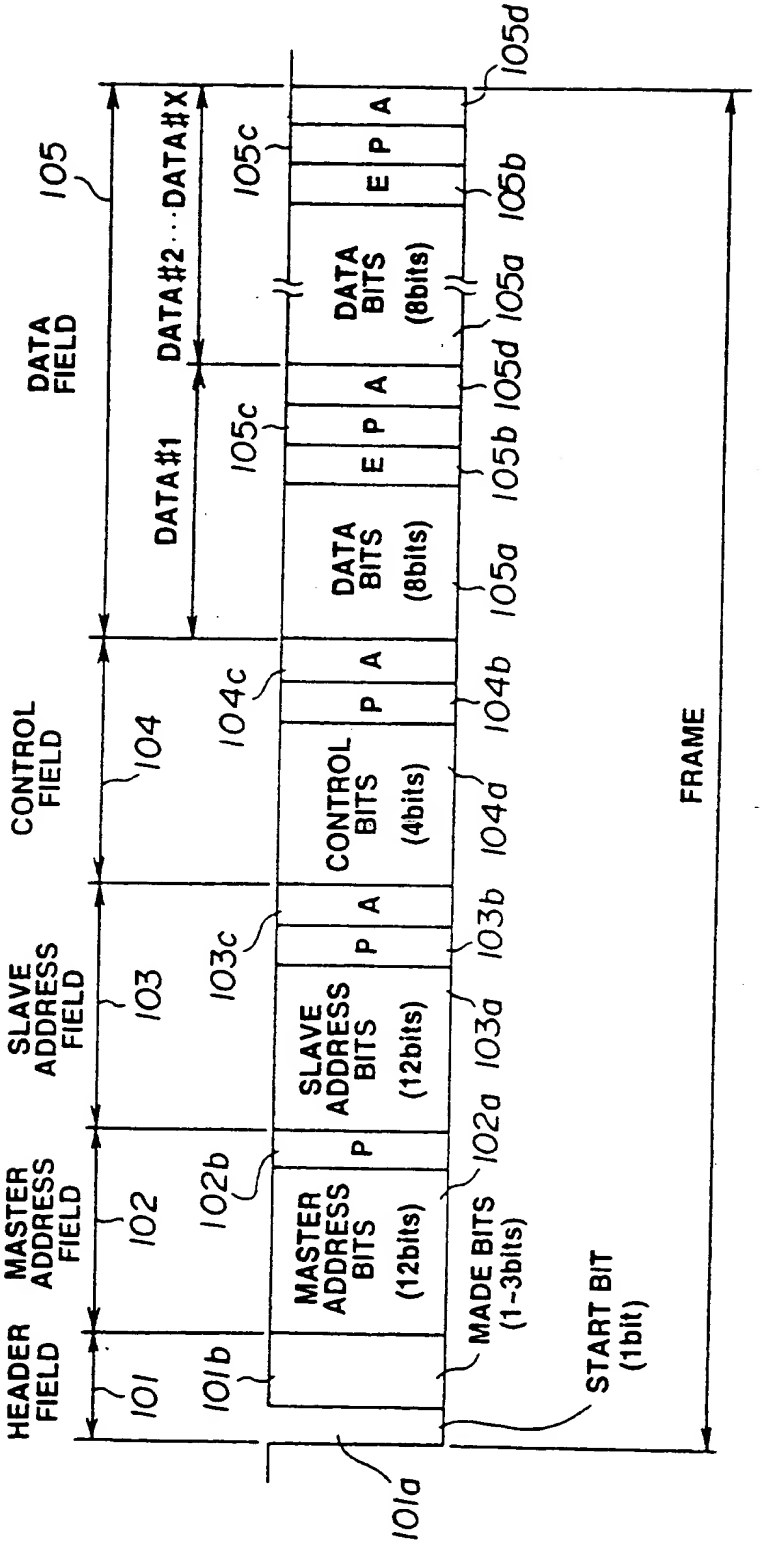


FIG.2

Bit number	Meaning
7	Always 0
6	Reserved for future standardization, "1"
5, 4	Source service code 00 ; CT 01 ; AV/C 10 ; HK 11 ; reserved
3, 2	Destination service code 00 ; CT 01 ; AV/C 10 ; HK 11 ; reserved
1	1/0 without/with SSDA
0	1/0 without/with DSDA

FIG.3

P1 (VTR → TV)

HEADER	HEADER
MASTER ADDRESS BITS	VTR
SLAVE ADDRESS BITS	TV
CONTROL BITS	DATA/ NON-LOCK
DATA #1 ⋮	DATA ⋮ DATA

P3 (VDP → TV)

HEADER
VDP
TV
DATA/ NON-LOCK
DATA ⋮ DATA

P2 (VTR → TV)

HEADER
VTR
TV
DATA/ NON-LOCK
DATA ⋮ DATA

FIG.4

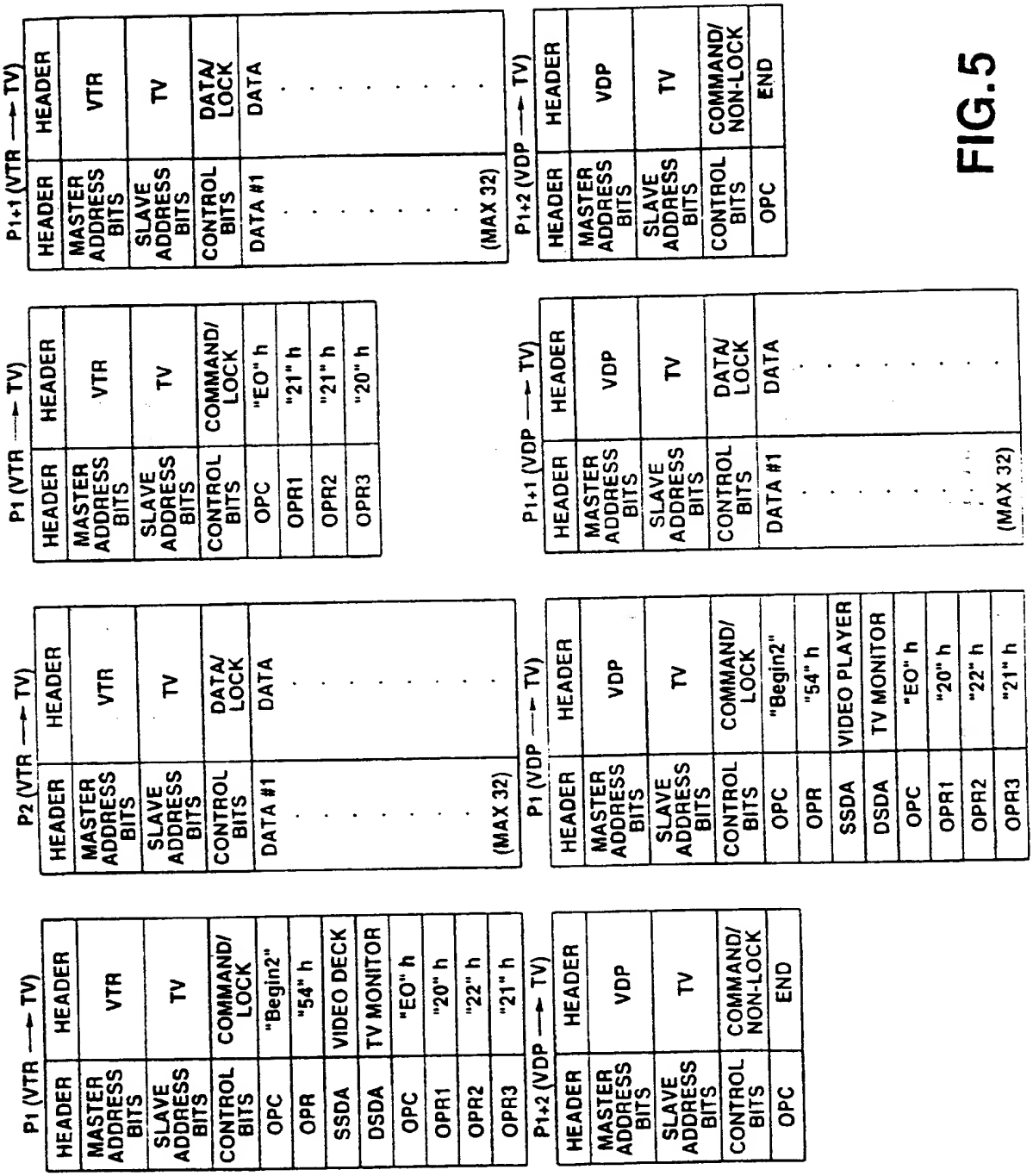


FIG.5

P1 (VTR → TV)

HEADER	HEADER
MASTER ADDRESS BITS	VTR
SLAVE ADDRESS BITS	TV
CONTROL BITS	COMMAND/ LOCK
OPC	"Begin2"
OPR	"54" h
SSDA	VIDEO DECK
DSDA	TV MONITOR
OPC	"EO" h
OPR1	"20" h
OPR2	"22" h
OPR3	"21" h

P2 (VTR → TV)

HEADER	HEADER
MASTER ADDRESS BITS	VTR
SLAVE ADDRESS BITS	TV
CONTROL BITS	DATA/ LOCK
DATA #1	DATA
.	.
.	.
.	.
.	.
.	.
.	.
.	.
.	.
(MAX 32)	

P3 (VTR → TV)

HEADER	HEADER
MASTER ADDRESS BITS	VTR
SLAVE ADDRESS BITS	TV
CONTROL BITS	COMMAND/ NON-LOCK
OPC	END

FIG.6

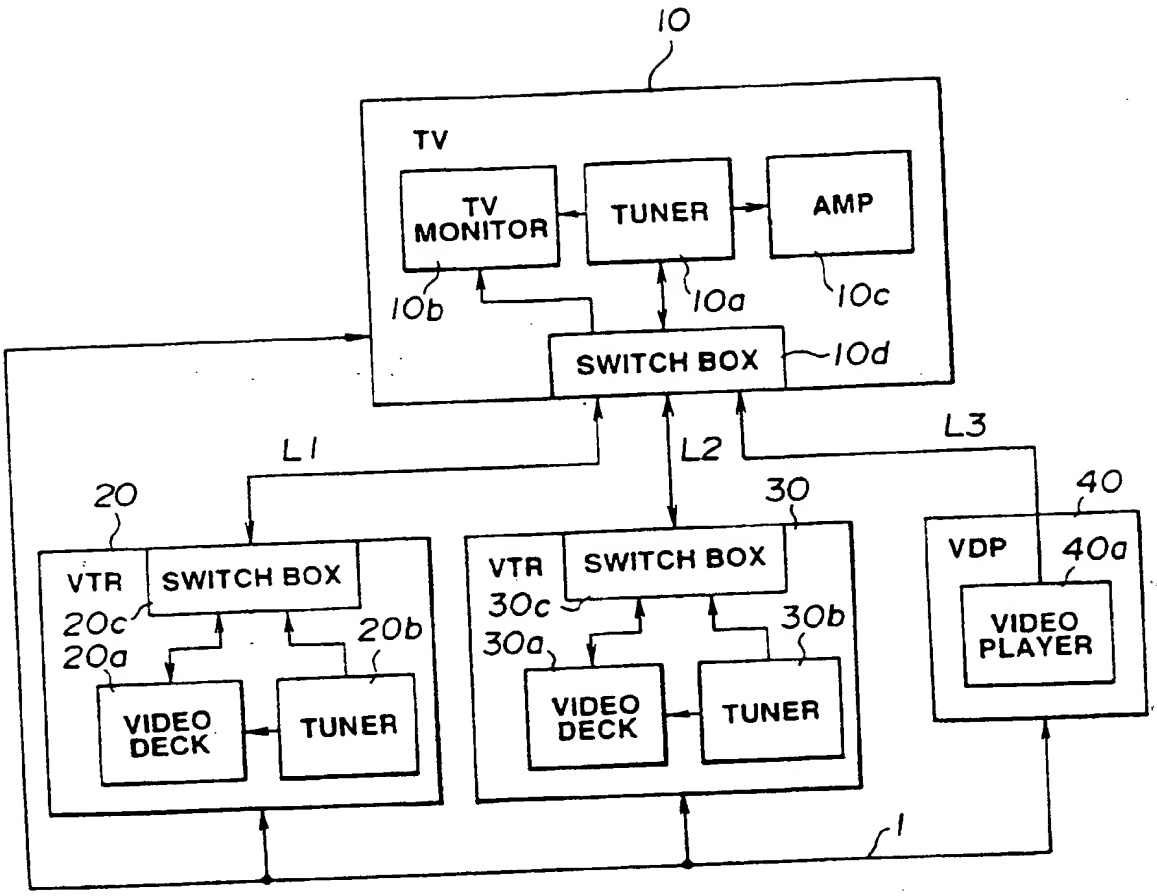


FIG.7

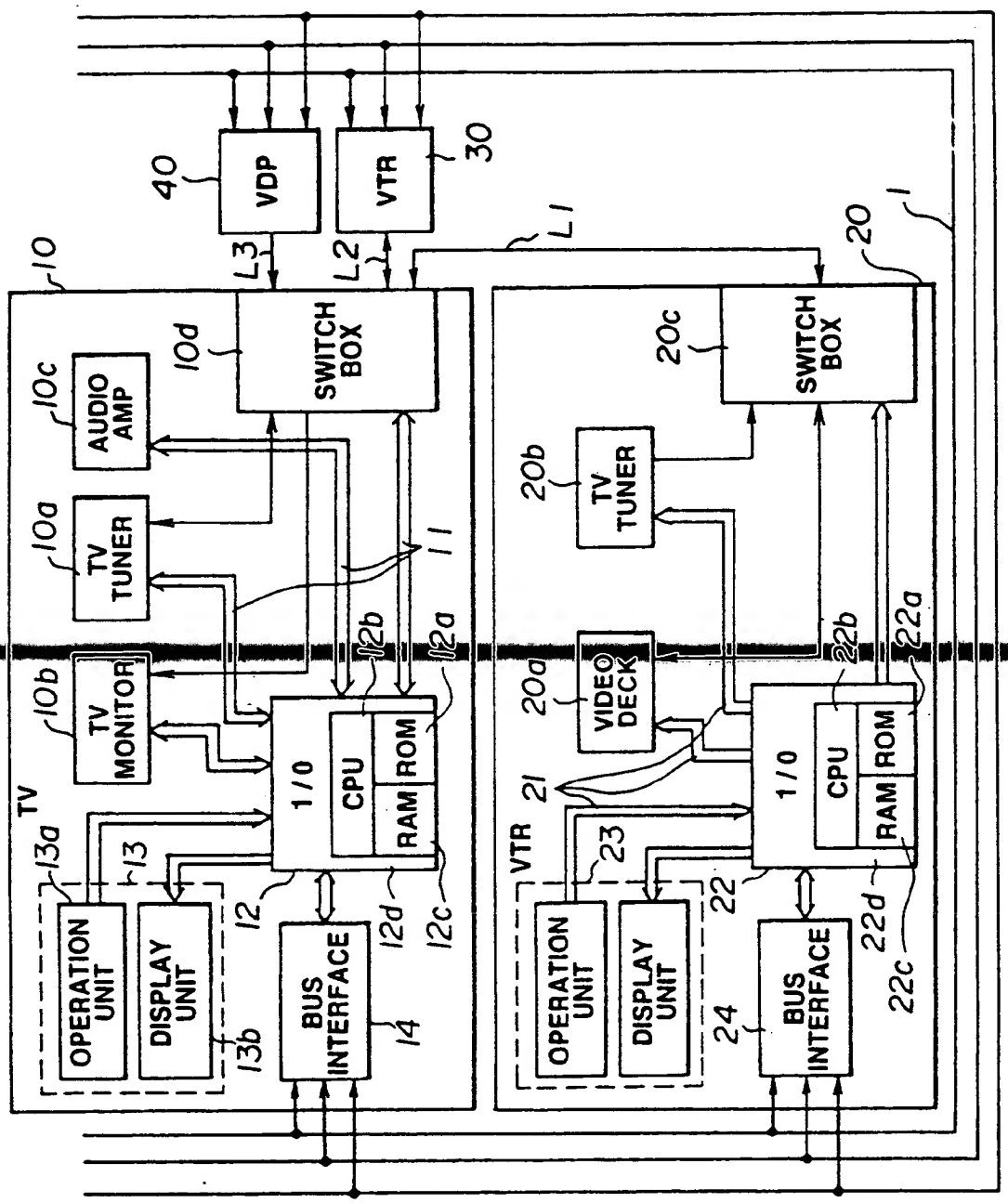


FIG.8

FIG.9 A

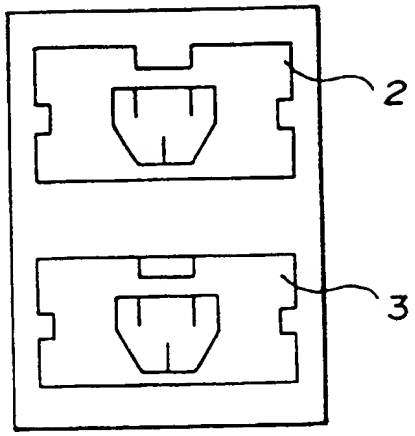
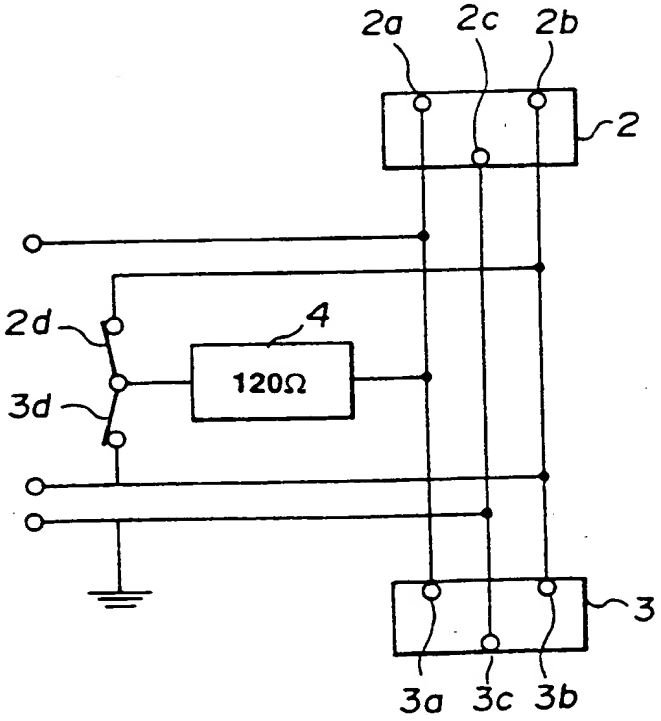


FIG.9 B



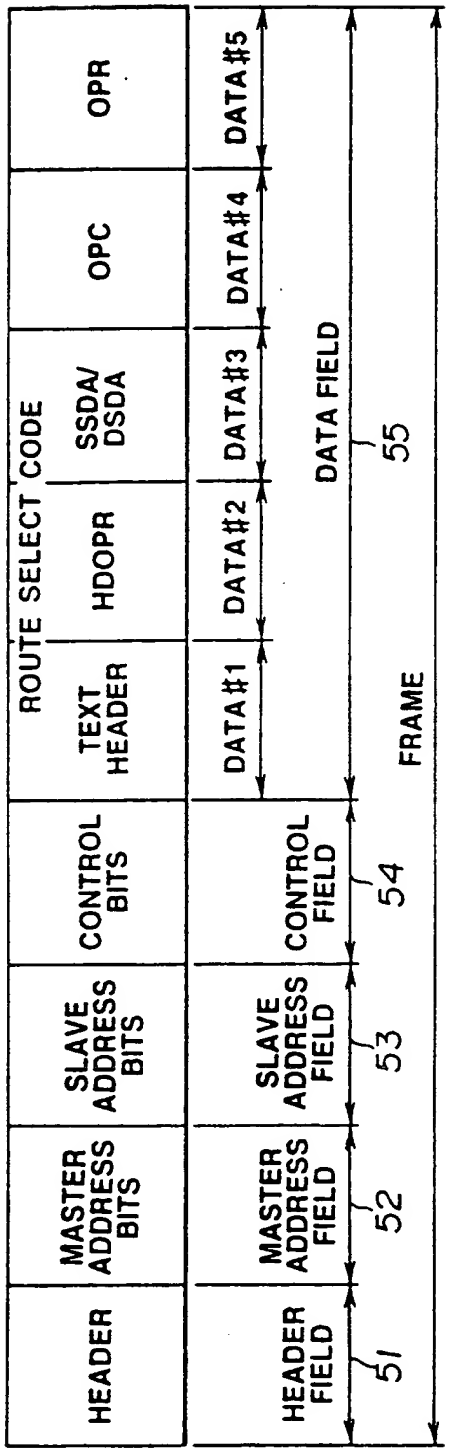


FIG.10

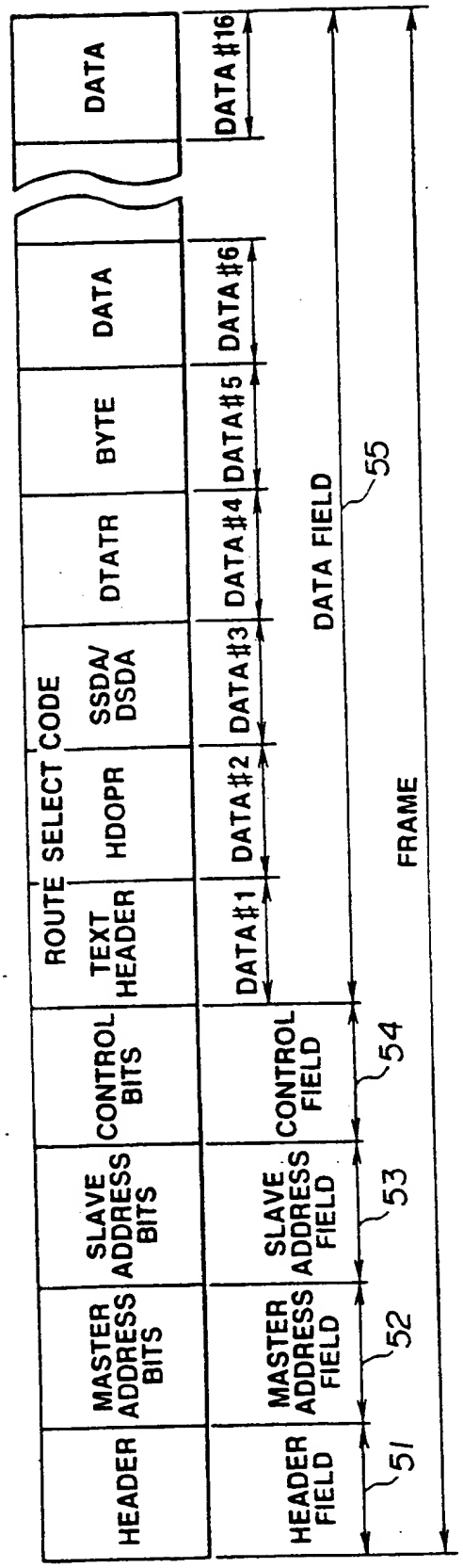


FIG.11

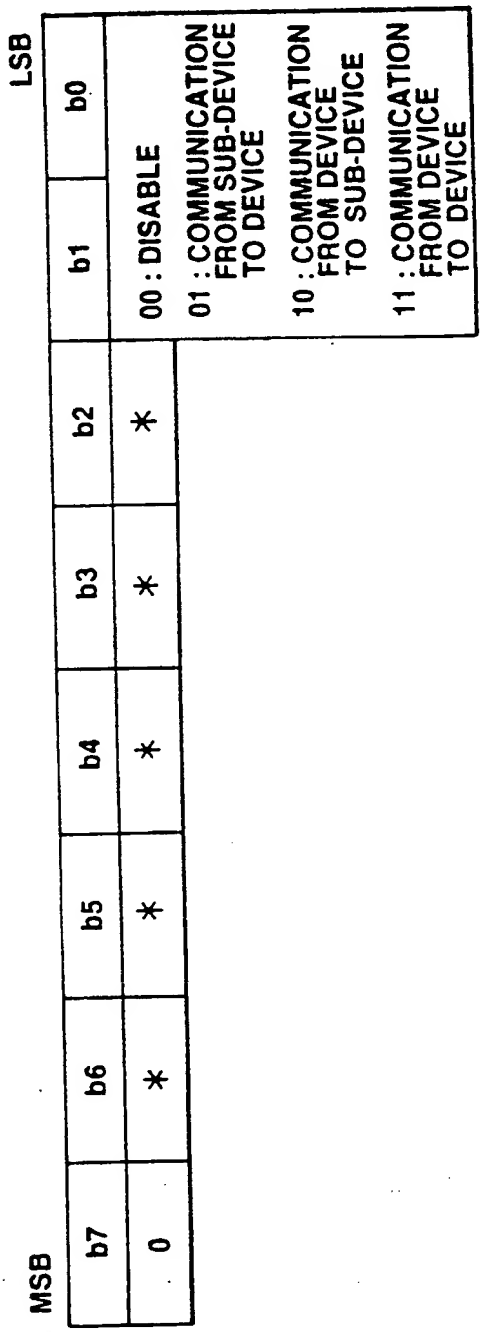


FIG.12

P1 (VTR → TV)

HEADER	HEADER
MASTER ADDRESS BITS	VTR
SLAVE ADDRESS BITS	TV
CONTROL BITS	DATA/ LOCK
TEXT HEADER	"AB" h
HDOPR	SUB-DEVICE → DEVICE
SSDA	VIDEO DECK
DTATR	"20" h
BYTE	"2A" h
OPR1	"20" h
OPR2	"22" h
OPR3	"21" h
DATA #9 ⋮ DATA #16	DATA ⋮ DATA

P2 (VTR → TV)

HEADER	HEADER
MASTER ADDRESS BITS	VTR
SLAVE ADDRESS BITS	TV
CONTROL BITS	DATA/ NON-LOCK
TEXT HEADER	"AB" h
HDOPR	SUB-DEVICE → DEVICE
SSDA	VIDEO DECK
DTATR	"20" h
BYTE	"27" h
DATA #6 ⋮ DATA #13	DATA ⋮ DATA

P3 (VDP → TV)

HEADER	HEADER
MASTER ADDRESS BITS	VDP
SLAVE ADDRESS BITS	TV
CONTROL BITS	DATA/ NON-LOCK
TEXT HEADER	"AB" h
HDOPR	SUB-DEVICE → DEVICE
SSDA	VIDEO PLAYER
DTATR	"20" h
BYTE	"2A" h
OPR1	"20" h
OPR2	"22" h
OPR3	"21" h
DATA #9 ⋮ DATA #16	DATA ⋮ DATA

FIG.13

P1 (VTR → TV)

HEADER	HEADER
MASTER ADDRESS BITS	VTR
SLAVE ADDRESS BITS	TV
CONTROL BITS	DATA/ NON-LOCK
TEXT HEADER	"AB" h
HDOPR	SUB-DEVICE → DEVICE
SSDA	VIDEO DECK
DTATR	"20" h
BYTE	"2A" h
OPR1	"20" h
OPR2	"21" h
OPR3	"20" h
DATA #9 ⋮ DATA #16	DATA ⋮ DATA

P2 (VDP → TV)

HEADER	HEADER
MASTER ADDRESS BITS	VDP
SLAVE ADDRESS BITS	TV
CONTROL BITS	DATA/ NON-LOCK
TEXT HEADER	"AB" h
HDOPR	SUB-DEVICE → DEVICE
SSDA	VIDEO PLAYER
DTATR	"20" h
BYTE	"2A" h
OPR1	"20" h
OPR2	"21" h
OPR3	"20" h
DATA #9 ⋮ DATA #16	DATA ⋮ DATA

FIG.14

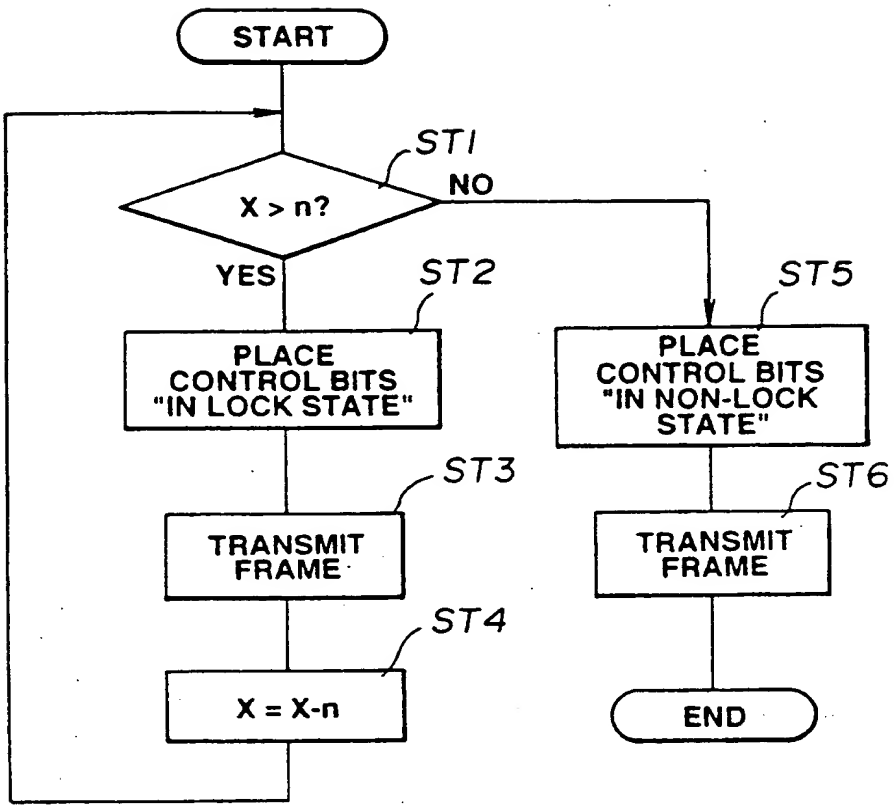


FIG.15

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 93 31 0316

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.5)
X	EP-A-0 350 838 (MATSUSHITA ELECTRIC INDUSTRIAL CO.) * column 1, line 4 - line 42 * * column 4, line 10 - column 5, line 34 *	1-8	H04B1/20 H04L12/40
X	EP-A-0 461 674 (NEC CORPORATION) * page 3, line 5 - line 25 * * page 6, line 30 - page 7, line 1; claims 3,6A,6B *	1,2,6	
A	EP-A-0 333 269 (N.V. PHILIPS' GLOEILAMPENFABRIEKEN) * claims *	1-8	

TECHNICAL FIELDS SEARCHED (Int.Cl.5)

H04B
H04L

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	6 April 1994	Goulding, C

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
A : technological background
O : non-written disclosure
P : intermediate document

T : theory or principle underlying the invention
E : earlier patent document, but published on, or after the filing date
D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document

EPO FORM 1503 03.82 (P04C01)

BEST AVAILABLE IMAGES

Defective images within this document are accurate representations of the original documents submitted by the applicant.

Defects in the images include but are not limited to the items checked:

- ☑ BLACK BORDERS
- ☐ IMAGE CUT OFF AT TOP, BOTTOM OR SIDES
- ☐ FADED TEXT OR DRAWING
- ☐ BLURRED OR ILLEGIBLE TEXT OR DRAWING
- ☐ SKEWED/SLANTED IMAGES
- ☐ COLOR OR BLACK AND WHITE PHOTOGRAPHS
- ☑ GRAY SCALE DOCUMENTS
- ☑ LINES OR MARKS ON ORIGINAL DOCUMENT
- ☐ REFERENCE(S) OR EXHIBIT(S) SUBMITTED ARE POOR QUALITY
- ☐ OTHER: _____

IMAGES ARE BEST AVAILABLE COPY.
As rescanning these documents will not correct the image problems checked, please do not report these problems to the IFW Image Problem Mailbox.